REMARKS

The Office Action of 07/28/2006 has been carefully considered. In response thereto, the claims have been amended as set forth above. Reconsideration and allowance in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-8 were rejected as being anticipated by Sakakibara. Claims 1, 2, 4, 5, 7 and 8 were rejected as being anticipated by Duboc. The claims have been amended to more clearly distinguish over the cited reference. Reconsideration is respectfully requested.

In particular, the claims have been amended to recite in part defining a set of memory addresses by an address configuration means using a base memory address and a configuration instruction for configuring the address configuration means; and transmitting a vector to/from a multi-port memory *at one time* using the set of memory addresses.

In Sakakibara, by contrast, a succession of addresses is defined using a single based address. This succession of addresses is not used to transmit a vector to/from a multi-port memory *at one time* as now recited in the claims.

The same distinction is believed to apply equally to Duboc.

4

Withdrawal of the rejections and allowance of claims 1-8 is respectfully requested.

Respectfully submitted,

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5